

ECE 600 Seminar  
Monday, November 14, 2011  
1610 Engineering Hall  
3:30PM - 5:00PM

## **CMOS Reliability Challenges in Nanometer-Scale Integrated Circuits**

### **Abstract**

As CMOS technologies have shrunk to the scale of tens of nanometers, reliability has emerged as a major challenge. The introduction of new technology paradigms such as 3D integration is excellent news for performance and enhanced integration, but such technologies are associated with increased thermal hotspots, which degrade system reliability.

There has been tremendous progress in developing new methods for modeling and diagnosing reliability at the level of individual transistors, but much less work on propagating these models to higher levels of abstraction, e.g., to predict the reliability of larger circuits. This talk will discuss research that develops computer-aided design techniques for estimating and enhancing the reliability of large logic circuits, with specific emphasis on failures due to phenomena such as bias temperature instability, gate oxide breakdown, and hot carrier injection, examining solutions that a circuit designer could practically apply to analyze or improve the lifetime of a design.

### **Bio**

Sachin Sapatnekar received his Ph.D. from the University of Illinois at Urbana-Champaign in 1992. He is currently at the University of Minnesota, where he holds the Distinguished McKnight University Professorship and the Henle Professorship in ECE. His research is related to developing CAD techniques for the analysis and optimization of circuit performance. He recently served as General Chair for the 2010 ACM/IEEE Design Automation Conference (DAC) and is currently Editor-in-Chief of the IEEE Transactions on CAD. He is a recipient of the NSF Career Award, six conference Best Paper awards, and the SRC Technical Excellence award, and is a fellow of the IEEE.