

ECE 600 Seminar
February 7, 2011, 3:45 – 4:45PM, EH 1800

Title: ***Robust Optimization of Digital Integrated Circuits: Progress and Challenges***

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Abstract:

This presentation will focus on the challenge of optimizing digital integrated circuits in the face of inevitable and increasing process variations. The talk will consist of three main parts. In the first part, a quick tutorial introduction to statistical timing analysis will be provided. Statistical timing is an efficient and accurate way of taking process variations into account during integrated circuit design. In the second part, recent work in continuous transistor sizing of custom digital macros by exploiting statistical timing will be described. In the final section, open challenges in discrete circuit optimization during physical synthesis will be formulated.

Biography:

Chandu Visweswariah obtained a PhD in Computer Engineering from Carnegie Mellon University. He was a Research Staff Member at the IBM Thomas J. Watson Research Center from 1989 to 2009. He is currently the Senior Manager of Timing and Circuit Analysis in the Electronic Design Automation (EDA) department of IBM Systems and Technology Group. He invented and developed several circuit analysis and optimization tools that are widely used in IBM.

Chandu is the author or co-author of one book and 98 publications; he holds 35 issued patents. In 2002, he was a visiting faculty member at the Eindhoven University of Technology in the Netherlands. He was profiled in the EE Times "Great Minds, Great Ideas" 2005 project focusing on disruptive innovation. His team won the EDN "Innovation of the Year (EDA Tools Category)" and "Innovator of the Year" awards in 2006 for work on statistical timing. Chandu has received numerous IBM Technical Achievement Awards, Best Paper awards and an IBM Corporate Award.

Chandu is a Fellow of the IEEE and a member of IBM's Academy of Technology. He was appointed an IBM Distinguished Engineer in 2009.