

ECE 600 Seminar
December 6, 2010, 3:45 – 4:45PM, EH 1610

Title: ***The Role of CAD in Solving Intel's Power/Performance Challenges: Past, Present and Future***

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Abstract:

Over the years, CAD has played a major role in solving design challenges encountered in scaling microprocessors to ever smaller dimensions and in deploying ever more complex high-performance architectures. Frequency was the main challenge for many years---then came the so called “right-hand” turn and power became an additional major focus, and then a constraint. We will present some of the CAD tools, technologies, and flows developed by SCL (Strategic CAD Labs) during this time period and how they were used in microprocessor development at Intel. We will then discuss how the product landscape at Intel is expanding into cell phones, netbooks, and other low cost devices and how that opens the door for new CAD opportunities. We will also introduce future research needs and directions (five to ten years out) that are suitable for academic/industrial collaboration.

Short Bio:

Steve Burns is a Senior Principal Engineer at Intel's Strategic CAD Labs (part of Design, Technology and Solutions) based in Hillsboro, OR. Steve has been working in this group for 14 years in the areas of: timing and race analysis for pulsed domino circuits, algorithms and methodology for sizing and power optimization of large synthesis and data-path blocks, transformation-based design environments, and advanced synthesis algorithms and methods. He currently leads the Power, Performance, and Technology team within Strategic CAD Labs and is responsible for the research roadmap in the Power/Performance domain for the Intel's CAD organization.