Title: FinFETs: Novel Circuit-Architecture Design Opportunities

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Abstract:

The constant march of miniaturization of transistors with each new generation of bulk CMOS technology has resulted in significant improvements in digital circuit performance. Further scaling of bulk CMOS, however, faces significant challenges due to fundamental material and process technology limits, including short-channel effects, subthreshold leakage, and device-to-device variations. The industry is moving towards FinFETs to overcome these obstacles to scaling.

In this talk, we will explore the novel design opportunities, from the circuit to architecture level, made possible by the double-gate nature of FinFETs. Independent control of the front and back gates of FinFETs as well use of asymmetric workfunctions enable various new logic styles. They also make fine-grain leakage-delay tradeoffs possible. This leads to designs that are not feasible in bulk CMOS. We will look at the impact of process-voltage-temperature (PVT) variations on FinFET circuits. We will also discuss a tool called FinCANON that enables the analysis of FinFET cache and network-on-chip under PVT variations. The tool is available for download from the speaker’s website.

Bio:

Niraj K. Jha received his B.Tech. degree in Electronics and Electrical Communication Engineering from Indian Institute of Technology, Kharagpur, India in 1981 and Ph.D. degree in Electrical Engineering from University of Illinois at Urbana-Champaign in 1985. He is a Professor of Electrical Engineering at Princeton University. He also serves as an Associate Director for the Princeton Andlinger Center for Energy and the Environment. He is a Fellow of IEEE and ACM. He has co-authored five books, among which are “Switching and Finite Automata Theory, 3rd ed.” and “Testing of Digital Systems” that are being used around the world. He has served as the editor-in-chief of IEEE Transactions on VLSI Systems and on the editorial boards of several other IEEE Transactions. He is a co-author of 14 award-winning papers. His research interests include FinFETs, power analysis and optimization, IC design automation, computer architecture, computer security, quantum computing, and energy-efficient buildings.